REMARKS

Reconsideration and allowance of the pending claims in the application are requested.

Claims 1-8 and 10-22 are in the case.

Claim 3 is objected to because of a typographical error.

Claims 22, 10-11 have been rejected u under 35 USC 112, second paragraph, as indefinite for failure to positively recite a "phase lock loop", as claimed.

Claim 12 has been rejected under 35 USC 112, second paragraph, because of an insufficient antecedent for the term "the phase locked loop" and the term "the transmitter".

Claims 1-8 and 21 have been rejected under 35 USC 103(a) as unpatentable over newly cited USP 5,774,450 to Harada et al., issued June 30, 1998 (Harada) in view of newly cited USP 5,812,523 to Isaksson et al., issued September 22, 1998 (Isaksson).

Claim 22, 10 and 11 are indicated as being allowable if rewritten or amended to overcome the rejection under 35 USC 112, second paragraph.

Before responding to the rejections, Applicants would like to distinguish Harada and Isaksson from the present invention (Cupo), as follows:

1. Harada discloses an orthogonal frequency division-multiplexing signal transmitted from a transmitting end to a receiving end. The transmitting end continuously transmits a first symbol (Sm) which includes data to be transmitted. The transmitting intermittently transmits a second symbol (SO) having a predetermined particular pattern every time a predetermined number of first symbols are transmitted. The symbol SO is used to correct the variation in the receiving level due to attenuation. The correction is done by detecting an envelope of received

data, correlating the analog signal with a stored single tone data corresponding to the particular pattern of the symbol SO. Based on the correlation, a control signal is generated that controls the gain of an automatic gain amplifier. Harada fails to disclose elements of Cupo, as follows:

A. Harada discloses generating a symbol SO with a particular pattern using the pattern to eventually generate a feedback and control signal that controls the gain of an automatic gain amplifier, which gain varies depending on the control signal for changing the levels of the received signal. In contrast, Cupo accurately determines the boundary of each OFDM plane, using a phase-lock loop. The frequency offset in each frame is corrected by taking a running average over the latest L-frames for correction of timing and frequency offset, as described in the specification at page 7, lines 17continuing to page 8, line 16. Harada corrects receiving signal levels and fails to disclose correcting timing and frequency offset in an OFDM

B. Harada takes the envelope of received data, compares this envelope or analog signal with a stored single toned data, corresponding to the particular pattern of the symbol SO. The comparison is used to generate a control signal that controls the gain of an automatic gain control amplifier to correct the received signal level. In contrast, Cupo discloses an offset estimator which estimates the offset as the negative of the phase angle of the auto correlation function for I and Q signal components at the frame boundary supplied by the phase lock loop. The estimated offset is provided to an offset correction circuit which corrects for frequency synchronization, frame synchronization and transmitter/receiver frequency offset, as described in the specification at page 8, lines 5 – 13. Harada discloses correcting for receiving level and variation in frequency band and fails to disclose fails to disclose frequency

synchronization, frame synchronization and transmitter/receiver frequency offset

2. Isaksson discloses an OFDM receiver, including an A/D converter for digitizing an OFDM signal and a synchronization means for performing a cross-correlation of the OFDM signal for outputting a frame clock. A phase-locked loop produces a synchronized digitized OFDM signal. A Fast Fourier transformer (FFT) processor arranges to receive the synchronized digitized OFDM signal based on the frame block, and de-multiplex the synchronized digitized OFDM signal. The phase lock loop retrieves the frame clock generating control signals for the FFT processor, the clock control signals indicating the point in time where to start sampling the OFDM symbol. A phase detector unit calculates the phase for the correlation maxima synchronously with the frame clock. A peak detector unit is triggered directly by the frame clock and calculates the phase at the point in time. The phase is directly proportional to the frequency error. Isaksson fails to disclose elements of Cupo, as follows:

A. Isaksson discloses a phase-lock loop producing a synchronized digitized OFDM signal for input to a FFT processor for demultiplexing a synchronized digitized OFDM signal. In contrast, Cupo discloses a digital phase-lock loop, which compares estimated frame boundaries for successive frames depending on the difference between the instantaneous frame values, a loop gain is dynamically adjusted in each symbol period. The differences are saved in a FIFO circuit and averaged over the eight latest frames and provided as the sample number for the desired frame boundary, as described in the specification at page 7, lines 17 - 25. Isaksson discloses a phase-lock loop producing a synchronized digitized OFDM signal for input to a FFT processor for demultiplexing a synchronized digitized OFDM signal and fails to disclose a phase

lock loop generating a sample number of a desired frame boundary for timing and frequency offset correction.

B. Isaksson discloses collecting sampled complex OFDM signals and splitting them into two branches. In one branch, the sample of the signal is delayed in a shift register. The other branch converts the signal into a real and imaginary part. The two branches are multiplied together in a complex multiplier. The output signal from the multiplier is again split into two branches. One branch is delayed in a shift register by "n" samples. The two signals are subtracted and integrated to form a filtered signal. A frame clock is formed from the absolute value of the two input signals. A phase lock loop retrieves the frame clock which generates control signals indicating the point in time for an FFT processor to start sampling an OFDM symbol. In contrast, Cupo filters the estimated frame synchronization differences for successive samples, averages the differences over the eight latest frames, filters the differences and rounds them off to the nearest integer indicative of the frame boundary. Isaksson discloses a frequency synchronization device for frequency error and fails to disclose a phase lock loop for frame synchronization..

Summarizing, Harada and Isaksson fail to disclose a phase lock loop providing a sample number indicating a framed boundary to an offset estimator, which selects an offset value as a negative of the phase angle of an auto correlation function as the frame number for demodulating data corrected for timing and frequency in an OFDM. Without such disclosure there is no basis for a worker skilled in the art to implement claims 1 –8, 10 –22 and the rejection under 35 USC 103 (a) fails for lack of support in the cited references. Withdrawal of the rejection and

allowance of claims 1-8 and 10-21 are requested.

In any case, the failure of the newly cited art to disclose the claimed invention, as described above, renders the final rejection premature which should be vacated and a non-final Office Action issued.

Now turning to the rejections, Applicants provide responses to the indicated paragraphs of the Office Action, as follows:

REGARDING PARAGRAPH 1:

Applicants note the Examiner's remarks.

REGARDING PARAGRAPH 2:

Applicants have amended claim 3 to replace the term "he" with "the" before the term "OFDM". Withdrawal of the objection to claim 3 is requested.

REGARDING PARAGRAPHS 3 & 4:

Claim 22 has been amended to include the term "phase lock loop" before the element of "means for providing a sample number indicating an OFDM frame boundary...". The amendment provides an antecedent for the description of the phase lock loop subsequently described in claim 22.

Withdrawal of the rejection under 35 USC 112/2 and allowance of claim 22 is requested.

Claims 10 and 11, which depend upon claim 22 are believed to allowable on the same basis as claim 22.

REGARDING PARAGRAPHS 5 & 6:

The terms "phase locked loop" and "the transmitter " do not appear in claim 12. However, the term "phase lock loop" appears in claim 12 as part of the preamble (lines 3 and 5) and is positively recited in the claim at line 12. The term "a transmitter" is described in the preamble (line 6) and in the claim at line 13 and 14 as "the transmitter". Applicants have amended claim 21 at line 13 to recite "a transmitter" as a positive element.

Entry of the amendment to overcome any rejection of claim 21 for indefiniteness

REGARDING PARAGRAPH 7 & 8:

Claims 1-8, 21 disclose elements not disclosed or suggested in Harada, in view of Isaksson, as follows:

a. Claims 1, 12 & 21:

(i) "means for computing auto correlation amplitude and phase values of the I and Q components at sample points;"

Harada, at col. 18, lines 10-15, describes a correlation detector previously stores information of an ideal frequency component with respect to a particular symbol SO, as a reference information. The correlation detector 81 finds the correlation between the reference information and data on the frequency axis outputted from FFT to output a correlation signal, as

shown in Fig. 10(a). In contrast, Cupo discloses in Figure 2A ,the I/Q components of a received signal are sampled in an A/D converter at 544 points using a receiver-sampling clock. The output of the converters is provided to a standard two-frame FIFO, which feeds into an offset correcting circuit and in a correlator 32. The correlator starting from the first sample in the FIFO, a complex auto correlation function is computed for each sample. See page 6, line 25 continuing to page 7, line 6. Harada correlates reference information stored in a correlation detector with data on the frequency access outputted from a foyer transformer and fails to disclose computing auto correlation amplitude and phase values of the I and Q components at sample points.

(ii) "means for averaging and saving the auto correlation values of the I and Q components over L symbols for two or more frames before computing the correlation;"

Harada, at col. 10, lines 42-60, describes the operation of the symbol energy detector (shown in Fig. 2) to find the energy of a symbol in terms of a digital value. The found energy digital value is converted into an analog value by a D/A converter to output an analog symbol energy symbol representing the energy of the symbol. Harada, at col. 10, lines 42-60, does not describe averaging and saving the auto correlation values of the I and Q components over L symbols before computing the correlation, as described in the specification at page 7, lines 6-10.

Harada, at col. 16, line 53-67, describes a frequency region energy detector 71 (shown in Fig. 7) to generate a frequency region energy signal, representative of a shift direction and the amount of shift from a center of frequency for a symbol. The shift direction and amount

of shift direction are used to correct the variation in the frequency band of OFDM signal. Harada discloses finding the energy level of a symbol and fails to disclose averaging auto correlation values of I and Q components over L symbols, before computing a correlation.

Harada, at col. 8, lines 10-40, discloses a correlation detector finds the sum of the results of the multiplication between the information to be detected and the reference information, while shifting the position of the information to be detected on a frequency access for each code. The set of sums becomes a correlation signal. The correlation signal exhibits a peak when respective correspondences between code information included in the information to be detected and code information included in the reference information coincides with each other on a frequency basis. Applicant can find no disclosure in Harada in averaging and saving auto correlation values before computing a correlation. Moreover, the correlation value in Harada comprises a set of sum of the results of the multiplication between information to be detected and reference information, while shifting the position of the information to be detected on the frequency access. In contrast, Cupo discloses the correlation value, based on the I and Q components, for computing a frame boundary as described in the specification at page 7, lines 6-9.

Harada fails to disclose averaging the auto correlation values of I and Q components over L symbols and saving them for computing a correlation factor, based on the auto correlation of the I and Q components.

(iii) "phase lock loop means for providing a sample number indicating an OFDM frame boundary using the average I and Q auto correlation values and an output signal

locked to the transmitter RF signal;"

The Examiner acknowledges that Harada does not disclose a phase lock loop providing a sample number indicating an OFDM frame boundary. The Examiner substitutes Isaksson disclosure which describes a feedback loop at col. 5, lines 39-55 and at col. 7, lines 34-35. Isaksson describes a phase lock loop for a generation of a frame clock to be used by a FFT processor symbol detection (Figure 1). Applicant can find no disclosure in Isaksson relating to a phase lock loop generating a sample number indicating an OFDM frame boundary for timing and frequency offset correction, as described in the specification at page 7, line 14-16. Moreover, Isaksson activates a phase lock loop which provides a frame clock to a phase detector unit, which calculates the phase of the sampled OFDM signals as representative of the frequency error. In contrast, the phase lock loop in Cupo provides an output to correct offset and remove the guard period by locking the output signal to the transmitter RF signal. Isaksson fails to disclose a phase lock loop generating a sample number indicated in OFDM frame number and providing an output signal locked to the transmitter RF signal.

Moreover, substitution of the Isaksson phase lock loop into Harada as a means for generating a clock signal activating a FFT processor for symbol detection would serve no useful purpose and would be in conflict with the Harada symbol pattern detection method

(iv) "means for providing a receiver clock chain output phase locked to the transmitter RF signal;"

Harada, at col. 10, lines 12-40 describes a symbol timing synchronizing circuit, which is synchronized with each of the symbols on the basis of a reference timing signal and

provides a symbol synchronizing signal to a clock terminal of a FFT and a correlator for generating a correlation signal . In contrast, Cupo discloses the digital phase lock loop provides an input to a programmable counter, responsive to a receiver clock and transmits a receiver clock chain phase locked to the transmitter clock. Applicants can find no disclosure in Harada of generating a receiver clock chain, which locks the receiver clock and transmitter clock.

(v) "means for providing an offset value indicative of the phase difference of a phase receiver and a transmitter;"

Isaksson at col. 5, lines 35 – 65 describes a synchronization block for determining frequency error between transmitter and receiver and generating a complex rotating vector multiplied by the received signal to compensate for frequency errors between receiver and transmitter. Harada discloses taking the difference in energy levels of guard symbols as a means for matching the receiving and transmitting power levels. Applicant can find no disclosure in Isaksson and Harada related to calculating an offset value indicative of the phase difference between the receiver and transmitter.

(vi) "means for correcting frequency and timing offset between the receiver and the transmitter in the sample number."

Harada at col. 4, lines 30 – 40; col.5, lines 52 – 60; col.6, lines 1 – 6 and col. 16, lines 1 – 19 describe correcting the variation in the receiving level on the basis of a received second symbol; correcting the variation in the frequency band on the basis of the received second symbol and a symbol is detected by a reference timing generator and the frequency discriminating signal of the symbol is used as a control signal for improving the precision of a

frequency converter. Applicant can find no disclosure in Isaksson and Harada generating a sample number for timing and frequency offset correction in an ODFM receiver based upon a sample number generated by a phase lock loop, as described in the specification at page 7, lines 10-16.

Summarizing, Harada and Isaksson, alone or in combination, fail to disclose, suggest or teach the elements of claims 1, 12 and 21, as described above. Without a teaching in Harada and Isaksson, alone or in combination, relating to the claimed elements described above, there is no basis for a worker skilled in the art to implement claims 1, 12 and 21. Withdrawal of the rejection under 35 USC 103 (a) and allowance of claims 1, 12 and 21 are requested.

b. Claim 2 & 13

(i) "The OFDM receiver of Claim 1 further comprising:

means for estimating frame synchronization of the OFDM frame boundary."

Isaksson, col. 2, lines 55-67, described compensating for frequency errors not estimating frame synchronization.

Without a disclosure in Harada or Isaksson relating to estimating frame synchronization, as described in the specification at page 7, lines 11-14, there is no basis for the rejection of claim 2 and 13 under 35 USC 103(a). Withdrawal of the rejection of claims 2 and 13 under 35 USC 103(a) and allowance thereof are requested.

In any case, claims 2 and 13, when combined with claims 1 and 12 are patentable on the same basis thereof.

c. Claims 3, 15 & 16:

(i) " The OFDM receiver of Claim 1 further comprising:

means for phase locking the transmitter and the receiver. "

The Examiner has not indicated in either Harada or Isaksson, any disclosure relating to phase locking the transmitter and receiver to achieve accurate synchronization. Harada discloses symbol pattern detection for correcting the variation in the frequency band between receiver and transmitter to be corrected with high precision. While, Isaksson describes correcting the variation in the receiving level and/or the variation of frequencies band of the received signal.

Without a disclosure in Harada and Isaksson relating to phase locking the transmitter and receiver, there is no support for the rejection of claims 3, 15 and 16 under 35 USC 103(a). Withdrawal of the rejection and allowance of claims 3, 15 and 16 are requested.

In any case, claims 3, 15 and 16, when combined with claims 1 and 12, are patentable on the same basis thereof.

d. Claim 4:

Claim 4 depends upon claim 1 and is patentable on the same basis thereof.

e. Claims 5 & 15:

(i) "The OFDM receiver of Claim 1 further comprising:

means responsive to the sample number and a negative phase angle of the auto correlation values for correcting for frequency synchronization, frame synchronization, and transmitter/receiver

frequency offset.

Harada, at col. 17, line 14, describes a sample and hold device receiving frequency region energy signal from a frequency energy detector. The frequency region energy symbol is held in the sample hold device to serve as a control signal to frequency converter. The amount of frequency shipped to a frequency converter varies depending upon the voltage level of the control signal fed from the sample hold device to increase or decrease the frequency received from the transmitter. In contrast, Cupo discloses an offset estimator and an offset correction circuit modifies the amplitude and phase of each sample stored in a FIFO to correct the frequency synchronization, frame synchronization and transmitter frequency offset. Harada's sample and hold circuit does not perform the function of an offset estimator, as described in the specification at page 8, lines 5-10. The rejection of claims 5 and 14 under 35 USC 103(a) is without support and fails to provide a worker skilled in the art any basis for implementing claims 5 and 14.

Withdrawal of the rejection of claims 5 and 14 under 35 USC 103(a) and allowance thereof are requested. In any case, claims 5 and 14, when combined with claims 1 and 12 are patentable on the same basis thereof.

f. Claim 6:

Claim 6 depends upon claim 1 and is patentable on the same basis thereof.

g. Claims 7 & 17:

(i) " The OFDM receiver of Claim 1 further comprising:

means for storing the sampled I and Q components coupled to the auto correlation means and a correcting means.

Harada, at col. 18, lines 10-40, describes an output of the FFT provided to a correlation detector 31C and a demodulated data detector. Applicants can find no disclosure in Harada providing the I and Q components to a correlator 32 and a correction circuit 30, as described in the specification at page 8, line 25 and continuing to page 9, line 6. for determining the correct frame boundary for timing and frequency offset correction

Without a disclosure in Harada relating to storing the sample I and Q components in an auto correlation means and a correcting means for frame boundary processing , there is no support for the rejection of claims 7 and 17 under 35 USC 103(a). Withdrawal of the rejection of claims 7 and 17 and allowance thereof are requested. In any case, claims 7 and 17, when combined with claims 1 and 12 are patentable on the same basis thereof.

h. Claims 8 & 18:

(i) " The OFDM receiver of Claim 1 further comprising:

means for storing the averaged auto correlation values coupled to an offset estimator and a frame synchronization estimator.

Harada discloses storing sampled I and Q components in a correlation detector. In contrast, Cupo discloses storing in a FIFO coupled to an offset estimator and a synchronizing estimator. Moreover, there would be no need in Harada to include an offset estimator and a frame synchronization estimator because Harada is directed to symbol pattern detection for

correcting variations in the receiving levels with respect to a transmitted level. In contrast, Cupo uses I and Q components for detection of frame boundaries for offset correction.

Without a disclosure in Harada relating to storing I and Q components in FIFO coupled to an offset estimator and a frame synchronization estimator, there is no support for the rejection of claims 8 and 18 under 35 USC 103(a). Withdrawal of the rejection and allowance of claims 8 and 18 are requested.

In any case, claims 8 and 18, when combined with claims 1 and 12 are patentable on the same basis thereof.

i. Claim 19:

(i) "The method of Claim 12 further compnsing the steps of:

adjusting the phase angle of each sample in a storing means by an amount proportional to "n" where "n" is counted from a correct frame boundary."

The Examiner has not cited no can Applicants find any text in Harada or Isaksson relating to adjusting the phase angle of a loop sample by an amount proportional to "n" where "n" is counted from the correct frame value, as described in the specification at page. 9, lines 4-6. Without such disclosure in Harada and Isaksson , there is no support for the rejection of claim 19 under 35 USC 103(a).

Withdrawal of the rejection of claim 19 and allowance thereof are requested.

In any case, claim 19, when combined with claim 1 and 12, further describes elements not shown in Harada and Isaksson, alone or in combination. Claims 12 and 19, when combined, are patentable over the cited art.

j. Claim 20:

(i) "The method of Claim 12 compnsing the step of:

averaging the auto-correlation values over frames in a storage device."

Harada's correlator detectors in Fig. 1 and Fig. 9 determine the correlation between reference information and data on the frequency axis outputted from the FFT stored information, as described at col. 18, lines 9-15. There is no disclosure in Harada relating to averaging the auto correlation values of the I and Q components, as described in the specification at page 6, line 29 and continuing to page 7, lines 9.

Without a disclosure in Harada averaging the auto correlation values, there is no support for the rejection of claim 20 under 35 USC 103(a). Withdrawal of the rejection of claim 20 and allowance thereof are requested.

REGARDING PARAGRAPH 9:

Claim 22 has been amended to include an antecedent for the term "phase lock loop". The amendment of claim 22 is believed to overcome the rejection of claim 22 under 35 USC 112, second paragraph. Withdrawal of the rejection of claim 22 and allowance thereof are requested.

REGARDING PARAGRAPH 10:

Claims 10 and 11 have been discussed in paragraph 4 and are believed to overcome the rejection under 35 USC 112, second paragraph. Withdrawal of the

rejection and allowance of claims 10 and 11 are requested.

REGARDING PARAGRAPH 11:

Applicants submit that in addition to the elements identified by the Examiner as not disclosed in Harada and Isaksson, Applicants points out:

(a) There is no disclosure relating to (a) means for averaging and saving the auto correlation values of the I and Q components with the L symbols for two or more frames before computing the correlation;

(b) A receiver clock chain output phase locked to the transmitter;

(c) an offset value indicative of a phase difference between the receiver and the transmitter;

(d) correcting frequency and timing offset between the receiver and the transmitter.

All of the foregoing elements have been discussed in connection with the consideration of claim 1 and are not shown, suggested or taught in Harada and Isaksson, taken alone or in combination.

CONCLUSION:

Having amended claim 22 to overcome the rejection under 35 USC 112, second paragraph and distinguished claims 1-8 and 10-21 from the cited art, entry of the amendment, allowance of the claims, passage to issue of the case are requested or, in the alternative, withdrawal of the final rejection as premature and issuance of a non-final Office Action are requested based on the failure of the newly cited art to disclose, suggest or teach the subject matter of claims 1 – 8 and 10 -22 as discussed above in connection with distinguishing claims 1 – 8 , and 10 – 22 from the newly cited art.

AUTHORIZATION:

The Commissioner is hereby authorized to charge any fees or insufficient fees or credit any payment or overpayment associated with this application to IBM Deposit Account No. 13-4503, Order No. 3037-4167 CUPO-20-2.

Respectfully submitted,

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Dated: D R A F T By:_____

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